METHODS OF DESIGNING A LAYOUT OF A SEMICONDUCTOR DEVICE INCLUDING FIELD EFFECT TRANSISTOR AND METHODS OF MANUFACTURING A SEMICONDUTOR DEVICE USING THE SAME

PRIORITY STATEMENT

[0001] This U.S. non-provisional patent application claims priority under 35 U.S.C. §119 to Korean Patent Applications No. 10-2015-0108171 and No. 10-2015-0157565, filed on Jul. 30, 2015 and Nov. 10, 2015, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] The inventive concept relates to the interconnections, such as metal lines and vias, of active elements a semiconductor device. More particularly, the inventive concept relates to a method of designing a layout of a semiconductor device including field effect transistors and to a method of manufacturing a semiconductor device using the same.

[0003] Due to their small-sized, multifunctional, and/or low-cost characteristics, semiconductor devices are esteemed in the electronics industry. Semiconductor devices may be classified as memory devices for storing data, logic devices for processing data, or hybrid devices including both of memory and logic elements. To meet an ever-increasing demand for electronic devices which operate at high speeds and/or consume low amounts of power, it is necessary to produce semiconductor devices that offer high performance and/or are multi-functional and yet remain highly reliable. To satisfy these technical requirements, the complexity and/or integration density of semiconductor devices is/are being increased.

SUMMARY

[0004] According to the inventive concept, there is provided a method of producing a layout of a semiconductor device, including providing a standard cell layout, the providing of the standard cell layout comprising creating a preliminary pin pattern of an interconnection layout of the standard cell layout, performing a routing step to produce a high-level interconnection layout in which a the preliminary pin pattern is connected to a high-level interconnection pattern, and generating a postliminary pin pattern in a region of the interconnection layout of the standard cell layout, based on hitting information obtained upon the completion of the routing step, and in which the postliminary pin pattern is smaller than the preliminary pin pattern.

[0005] According to the inventive concept, there is also provided a method of designing a layout of a semiconductor device may include providing a first standard cell layout and a second standard cell layout in a cell library, the providing of the first and second standard cell layouts including laying out a first preliminary pin pattern and a second preliminary pin pattern on the first and second standard cell layouts, respectively, laying out the first and second standard cell layouts, performing a routing step to connect the first and second preliminary pin patterns to high-level interconnection layouts, and generating a first pin pattern and a second pin pattern using the first and second preliminary pin patterns, respectively, based on hitting information to be obtained after the routing step. The first and second preliminary pin patterns may be the same as each other in terms of size and arrangement, and the first and second pin patterns may be different from each other in terms of size and arrangement.

[0006] According to the inventive concept, there is also provided a method of fabricating a semiconductor device, including a process of generating a layout of a semiconductor device, the layout comprising a standard cell layout, manufacturing a photomask having a mask pattern based on the layout of the semiconductor device, and forming layers of metal lines and vias on a substrate using the photomask, the vias vertically connecting different layers of the metal lines, and in which the generating of the layout of the semiconductor device comprises: laying out a lower via pattern on a logic layout of the standard cell layout, laying out a preliminary pin pattern on the lower via pattern, performing a routing step on the standard cell layout, which places a high-level interconnection layout and an upper via pattern on the preliminary pin pattern, the upper via pattern connecting the preliminary pin pattern to an element of the high-level interconnection layout, and generating a postliminary pin pattern connecting the lower via pattern to the upper via pattern, wherein the postliminary pin pattern and the preliminary pin pattern occupy overlapping regions in the process.

[0007] According to the inventive concept, there is also provided a method of fabricating a semiconductor device, including a process of generating a device layout of a semiconductor device, and manufacturing a semiconductor device using the device layout. The process of generating the device layout includes: acquiring a standard cell layout that includes a layout of active elements and/or regions of the semiconductor device, and an interconnection layout including a preliminary pin pattern defining a region in the semiconductor device containing a location of a lower via to be electrically connected to at least one of the active components and/or regions, performing a routing step comprising overlaying a high-level interconnection pattern and an upper via pattern on the standard cell layout, wherein the high-level interconnection pattern intersects the preliminary pin pattern and is representative of a high-level interconnection of the semiconductor device, and the upper via pattern is placed at the intersection of the high-level interconnection pattern and the preliminary pin pattern and represents the location of an upper via of the semiconductor device, producing hitting information indicative of the location of the upper via based on the routing step, and using the hitting information to produce a postliminary pin pattern representative of a region in the semiconductor device containing both the lower via and the upper via. The manufacturing of the semiconductor device comprises: forming active elements and/or regions at an upper part of a substrate as laid out based on the standard cell layout, forming layers of metal lines one above another on the substrate, and forming vias connecting the layers of metal lines to the active components, wherein the layers of metal lines comprise a lower level metal layer including a lower level metal interconnection corresponding to the postliminary pin pattern and an upper level metal layer including an upper level metal interconnection corresponding to the high-level interconnection, and the vias include a first via corresponding to the lower via and interposed between and